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2 **A tool for injecting SEU-like faults into the configuration control mechanism of Xilinx Virtex FPGAs**
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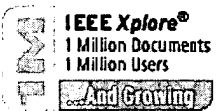| config* and bitstream* | **Search** |

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17	X		US 20010001881 A1	20010524	37	Methods and media for utilizing symbolic expressions in circuit modules
18	X		US 6817006 B1	20041109	28	Application-specific testing methods for programmable logic devices
19	X		US 6817005 B2	20041109	26	Modular design method and system for programmable logic devices
20	X		US 6802026 B1	20041005	8	Parameterizable and reconfigurable debugger core generators

21	X		US 6747478 B2	20040608	17	Field programmable gate array with convertibility to application specific integrated circuit

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
11	713/100			Nollet, Vincent et al.					
12	326/39			Madurawe, Raminda U.					
13	327/115			Nguyen, Andy T.					
14	719/328			Palem, Krishna et al.					
15	713/1	713/100; 713/501; 713/600		Trimberger, Stephen M. et al.					
16	716/18	716/7		Mason, Jeffrey M. et al.					
17	716/1	716/12; 716/13; 716/14		Mohan, Sundararajarao et al.					
18	716/16	716/17; 716/18		Wells; Robert W. et al.					
19	716/16	716/7; 716/8		Mason; Jeffrey M. et al.					
20	714/35	712/227		Patterson; Cameron D. et al.					

| 21 | 326/39 | 326/101;
326/47 | | Madurawe; Raminda
U. | | | | | | |

	4	5	Image Doc. Displayed	PT
11			US 20040049672	
12			US 20040004496	
13			US 20030107415	
14			US 20020174266	
15			US 20020010853	
16			US 20010047509	
17			US 20010001881	.
18			US 6817006	
19			US 6817005	
20			US 6802026	

21			US 6747478	

	U	1	Document ID	Issue Date	Pages	Title
22	X		US 6744816 B1	20040601	10	Video coding and decoding methods
23	X		US 6714057 B2	20040330	25	Multi-purpose digital frequency synthesizer circuit for a programmable logic device
24	X		US 6711674 B1	20040323	11	Method of watermarking configuration data in an FPGA by embedding the watermark corresponding to a macro obtained upon encountering a first watermark tag from the macro
25	X		US 6678646 B1	20040113	12	Method for implementing a physical design for a dynamically reconfigurable logic circuit
26	X		US 6651238 B1	20031118	21	Providing fault coverage of interconnect in an FPGA
27	X		US 6600788 B1	20030729	17	Narrow-band filter including sigma-delta modulator implemented in a programmable logic device
28	X		US 6594610 B1	20030715	11	Fault emulation testing of programmable logic devices
29	X		US 6510548 B1	20030121	9	Method for providing pre-designed modules for programmable logic devices

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
22	375/240			Park; Dong-seek et al.					
23	327/115	327/117; 377/47		Nguyen; Andy T.					
24	713/1	713/100; 713/168; 713/176; 713/2		Burnham; James L.					
25	703/22	703/24; 703/25; 716/5; 716/7; 716/8		McConnell; David A. et al.					
26	716/16	716/17; 716/4; 716/5		Wells; Robert W. et al.					
27	375/245	375/232; 375/243; 375/247		Dick; Christopher H. et al.					
28	702/117	702/123; 702/183; 702/58; 703/14; 703/27; 714/2; 714/30; 714/39; 714/725; 716/17; 716/4		Toutounchi; Shahin et al.					
29	716/16	716/17		Squires; David B.					

	4	5	Image Doc. Displayed	PT
22			US 6744816	
23			US 6714057	
24			US 6711674	
25			US 6678646	
26			US 6651238	
27			US 6600788	
28			US 6594610	
29			US 6510548	

	U	1	Document ID	Issue Date	Pages	Title
30	X		US 6510547 B1	20030121	8	Method and apparatus for evolving an object using simulated annealing and genetic processing techniques
31	X		US 6487648 B1	20021126	20	SDRAM controller implemented in a PLD
32	X		US 6480954 B2	20021112	86	Method of time multiplexing a programmable logic device
33	X		US 6457164 B1	20020924	38	Hetergeneous method for determining module placement in FPGAs
34	X		US 6453456 B1	20020917	12	System and method for interactive implementation and testing of logic cores on a programmable logic device
35	X		US 6351143 B1	20020226	15	Content-addressable memory implemented using programmable logic
36	X		US 6305005 B1	20011016	10	Methods to securely configure an FPGA using encrypted macros
37	X		US 6301695 B1	20011009	9	Methods to securely configure an FPGA using macro markers
38	X		US 6292925 B1	20010918	38	Context-sensitive self implementing modules
39	X		US 6278289 B1	20010821	14	Content-addressable memory implemented using programmable logic

40	X		US 6263430 B1	20010717	86	Method of time multiplexing a programmable logic device

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
30	716/16	345/419; 700/103; 706/13; 709/203		Levi; Delon					
31	711/167	326/39; 713/400; 713/503; 716/16		Hassoun; Joseph H.					
32	713/1	713/100; 713/501; 713/600		Trimberger; Stephen M. et al.					
33	716/8	716/10; 716/16; 716/18; 716/9		Hwang; L. James et al.					
34	716/16	716/17		Price; Timothy O.					
35	326/40	365/49; 711/108		Guccione; Steven A. et al.					
36	716/16	713/1; 713/100; 713/202; 716/18		Burnham; James L.					
37	716/16	713/1; 713/100; 716/17		Burnham; James L. et al.					
38	716/8	716/10; 716/14; 716/17; 716/2; 716/9; 719/315		Dellinger; Eric F. et al.					
39	326/40	326/39; 326/41		Guccione; Steven A. et al.					

40	713/1	713/100; 713/501; 713/600		Trimberger; Stephen M. et al.					

	4	5	Image Doc. Displayed	PT
30			US 6510547	
31			US 6487648	
32			US 6480954	
33			US 6457164	
34			US 6453456	
35			US 6351143	
36			US 6305005	
37			US 6301695	
38			US 6292925	
39			US 6278289	

40		US 6263430	

	U	1	Document ID	Issue Date	Pages	Title
41	X		US 6260182 B1	20010710	37	Method for specifying routing in a logic module by direct module communication
42	X		US 6243851 B1	20010605	37	Heterogeneous method for determining module placement in FPGAs
43	X		US 6216258 B1	20010410	39	FPGA modules parameterized by expressions
44	X		US 6212650 B1	20010403	11	Interactive dubug tool for programmable circuits
45	X		US 6144933 A	20001107	12	Method and apparatus for remotely probing and stimulating a programmable logic device
46	X		US 6011663 A	20000104	165	Digital VTR increasing recorded amount of high priority data
47	X		US 5995744 A	19991130	11	Network configuration of programmable circuits
48	X		US 5978260 A	19991102	89	Method of time multiplexing a programmable logic device
49	X		US 5959881 A	19990928	85	Programmable logic device including configuration data or user data memory slices
50	X		US 5838954 A	19981117	85	Computer-implemented method of optimizing a time multiplexed programmable logic device

51	X		US 5825662 A	19981020	85	Computer-implemented method of optimizing a time multiplexed programmable logic device

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
41	716/12	716/13; 716/14; 716/16		Mohan; Sundararajarao et al.					
42	716/10	716/1; 716/16; 716/17; 716/18; 716/21; 716/8; 716/9; 717/116; 717/118		Hwang; L. James et al.					
43	716/17	716/16; 716/18		Mohan; Sundararajarao et al.					
44	714/32	714/31; 714/38		Guccione; Steven A.					
45	703/23	703/28		Guccione; Steven A.					
46	360/48	386/109; 386/68; 386/73		Inoue; Sadayuki et al.					
47	703/23	713/100; 717/176		Guccione; Steven A.					
48	365/182	365/189.01		Trimberger; Stephen M. et al.					
49	365/182	365/51; 365/63		Trimberger; Stephen M. et al.					
50	716/16			Trimberger; Stephen M.					

| 51 | 716/3 | 326/39;
326/40;
716/16 | | Trimberger; Stephen M. | | | | | |

	4	5	Image Doc. Displayed	PT
41			US 6260182	
42			US 6243851	
43			US 6216258	
44			US 6212650	
45			US 6144933	
46			US 6011663	
47			US 5995744	
48			US 5978260	
49			US 5959881	
50			US 5838954	

51			US 5825662	

	U	1	Document ID	Issue Date	Pages	Title
52	X		US 5787007 A	19980728	9	Structure and method for loading RAM data within a programmable logic device
53	X		US 5784313 A	19980721	86	Programmable logic device including configuration data or user data memory slices
54	X		US 5778439 A	19980707	85	Programmable logic device with hierarchical configuration and state storage
55	X		US 5761484 A	19980602	17	Virtual interconnections for reconfigurable logic systems
56	X		US 5761483 A	19980602	85	Optimizing and operating a time multiplexed programmable logic device
57	X		US 5701441 A	19971223	85	Computer-implemented method of optimizing a design in a time multiplexed programmable logic device
58	X		US 5646545 A	19970708	89	Time multiplexed programmable logic device
59	X		US 5629637 A	19970513	87	Method of time multiplexing a programmable logic device
60	X		US 5600263 A	19970204	85	Configuration modes for a time multiplexed programmable logic device
61	X		US 5596742 A	19970121	15	Virtual interconnections for reconfigurable logic systems
62	X		US 5583450 A	19961210	88	Sequencer for a time multiplexed programmable logic device

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
52	716/16	326/39; 326/41; 703/23		Bauer; Trevor J.					
53	365/182	365/156		Trimberger; Stephen M. et al.					
54	711/153	711/117; 711/156; 711/173		Trimberger; Stephen M. et al.					
55	716/16			Agarwal; Anant et al.					
56	716/2	326/40; 326/41		Trimberger; Stephen M.					
57	716/16	326/39; 326/41		Trimberger; Stephen M.					
58	326/38	326/40		Trimberger; Stephen M. et al.					
59	326/93	326/38; 326/46		Trimberger; Stephen M. et al.					
60	326/39	326/41; 326/93		Trimberger; Stephen M. et al.					
61	716/16			Agarwal; Anant et al.					
62	326/41	326/40; 326/93		Trimberger; Stephen M. et al.					

	4	5	Image Doc. Displayed	PT
52			US 5787007	
53			US 5784313	
54			US 5778439	
55			US 5761484	
56			US 5761483	
57			US 5701441	
58			US 5646545	
59			US 5629637	
60			US 5600263	
61			US 5596742	
62			US 5583450	

	U	1	Document ID	Issue Date	Pages	Title
63	X		US 5068603 A	19911126	68	Structure and method for producing mask-programmed integrated circuits which are pin compatible substitutes for memory-configured logic arrays

	Current OR	Current XRef	Retrieval Classif	Inventor	S	C	P	2	3
63	714/726	257/E23.151 ; 257/E27.105		Mahoney; John E.					

	4	5	Image Doc. Displayed	PT
63			US 5068603	